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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/728,519

12/05/2003

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YOR920030526US1  
(17107)

9033

7590

03/02/2005

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EXAMINER

DANG, PHUC T

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/728,519

Applicant(s)

BEDELL ET AL.

Examiner

PHUC T. DANG

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2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 05 December 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-69 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) See Continuation Sheet is/are rejected.
- 7) ☒ Claim(s) 2, 5, 7, 8, 10, 14, 16-18, 22, 27, 30, 32, 33, 38, 40-42, 46, 51, 53, 54, 58, 60-62 and 66 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

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## **DETAILED ACTION**

### **Oath/Declaration**

1. The oath/declaration filed on December 5, 2003 is acceptable.

### **Specification**

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### **Claim Objections**

3. Claims 16, 40 and 60 are objected to because of the following informalities:

In claims 16, 40 and 60, line 1, the term "discloation" should change to --  
dislocation --.

### **Claim Rejections - 35 USC § 103**

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3-4, 6, 9, 11-13, 15, 19-21, 23-25, 26, 28-29, 31, 34, 36-37, 39, 43-45, 47-50, 52-53, 55-57, 59, 63-65 and 67-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen et al., hereinafter "Cohen" (Patent No. 6,774,015 B1).

Regarding claims 1, 3-4, 11, 15, 19, 23, 28-29, 36, 39, 43, 47, 50, 52, 55, 59, 63 and 67, Cohen discloses a method of fabricating a strained Si-on-insulator (SSOI) comprising the steps of:

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forming a Ge-containing layer (110, Fig. 2) that is strained on a surface of a Si-containing layer (100, Fig. 2), the Si-containing layer is located atop an insulating layer (150, Fig. 2) of a preformed silicon-on-insulator (SOI) substrate (160, Fig. 2);

subjecting the preformed SOI substrate containing the Ge-containing to a first annealing step [col. 5, lines 1-16];

performing an amorphization ion implantation (200, Fig. 3) to create a buried amorphized region (100', Fig. 4) comprising the entirety of the Si-containing layer and a lower portion of the Ge-containing layer (Fig. 4) [col. 5, lines 8-17];

subjecting the preformed SOI substrate containing the Ge-containing layer and the buried amorphized region to a second annealing step sufficient to recrystallize the buried amorphized region resulting in the Si-containing layer recrystallizing in a strained state [col. 5, lines 32-65]; and

selectively removing the Ge-containing layer providing a strained Si-containing-on-insulator substrate [Fig. 7].

Cohen discloses all the features of the claimed invention as discussed above, but does not disclose the temperature that the first and second annealing steps are performed in the process is from 600°C to 1100°C.

The temperature that the first and second annealing steps are performed in the process is considered to be obvious in a design of choice, since annealing steps usually performed after heating any semiconductor layer. Thus, it would have been obvious to one having ordinary skilled in the art at the time the invention was made to modify the teaching of Cohen by the above limitation for a purpose of improving the process.

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Claim 26 including claims 12 and 56 is similar to claims 1 and 50 above, except for an additional step of performing a defect creating ion implantation to create defects within or near the first crystalline semiconductor layer as suggested by Cohen in col. 4, lines 64-67.

Regarding claims 6 and 31, Cohen discloses the second crystalline semiconductor layer comprises Si, SiC, SiGe, SiGeC, Ge, GaAs, InAs, InP, another III/V or II/VI compound Semiconductor [Fig. 2].

Regarding claims 9 and 34, Cohen discloses forming the second crystalline semiconductor layer comprises an epitaxial growth process [Abstract].

Regarding claims 13 and 57, Cohen discloses the defect creating ion implantation is carried out using ions of hydrogen, deuterium, helium, oxygen, neon, boron, silicon or mixtures and isotopes thereof [col. 3, lines 13-15].

Regarding claims 20, 44 and 64, Cohen discloses the first annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process of a spike anneal [col. 3, lines 8-13].

Regarding claims 21, 45 and 65, Cohen discloses the amorphization ion implantation is carried out using ions selected from Si, P, As, Ge, C and any combination thereof [col. 5, lines 12-17].

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Regarding claims 24, 48 and 68, Cohen discloses the second annealing step is carried out using a rapid thermal annealing process, a furnace annealing process, a laser annealing process of a spike anneal [col. 3, lines 8-13].

Regarding claims 25, 39 and 69, Cohen discloses the selectively removing comprises chemical etching, reactive ion etching, low-temperature oxidation, atomic oxidation, chemical mechanical polishing, gas-cluster beam thinning or any combination thereof [col. 5, lines 59-65].

5. Cohen discloses the claimed invention except for the process parameters as claimed in claims 3, 15, 28, 39, 52 and 59. However, the selection of the claimed process parameters would have been obvious to one having ordinary skill in the art at the time the invention was made to improve the process, since it is well settled that when the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

#### **Allowable Subject Matter**

6. The following is a statement of reason for the indication of allowable subject matter:

Claims 2, 5, 7-8, 10, 14, 16-18, 22, 27, 30, 32-33, 38, 40-42, 46, 51, 53-54, 58, 60-62 and 66 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

None of the Prior Art made of record discloses the insulating layer is a crystalline or non-crystalline oxide or nitride that is highly resistant to Ge diffusion as cited in claims 2, 27

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and 51 and the first crystalline semiconductor layer is a Si-containing semiconductor as cited in claims 5 and 30 and the second crystalline semiconductor layer is a Ge-containing material as cited in claims 7 and 32 and the Ge-containing material is a SiGe alloy or pure Ge as cited in claims 8, 33 and 53 and the epitaxial growth process is selected from rapid thermal chemical vapor deposition, low-pressure chemical vapor deposition, ultra-light vacuum chemical vapor deposition, atmospheric pressure chemical vapor deposition, molecular beam epitaxy and plasma-enhanced chemical vapor deposition as cited in claims 10 and 54 and the ions are hydrogen or oxygen ions as cited in claims 14, 38 and 58 and the defects can serve as efficient dislocation nucleation sites which allow the second crystalline semiconductor layer to relax more efficiently as cited in claims 16, 40 and 60 and the defect creating ion implantation is performed using an implantation mask as cited in claims 17, 41 and 61 and the first annealing step is performed in an inert gas ambient or a forming gas ambient as cited in claims 18, 42 and 62 and the second annealing step is performed in an inert gas ambient or a forming gas ambient as cited in claims 22, 46 and 66.

### Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuc T. Dang whose telephone number is (571) 272-1776. The examiner can normally be reached on 8:00 am-5:00 pm.
8. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone numbers

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for the organization where this application or proceeding is assigned are 703-872-9306

for regular communications and After Final communications.

9. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Phuc T. Dang

PP

A handwritten signature in black ink, appearing to read 'Phuc T. Dang', written in a cursive style.

Primary Examiner

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Continuation of Disposition of Claims: Claims rejected are 1,3,4,6,9,11-13,15,19-21,23-26,28,29,31,34-37,39,43-45,47-50,52,55-57,59,63-65 and 67-69.